	Type	L #	Hits	Search Text	DBs
1	BRS	L1	9	cho near in-wook.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L2	95	lee near nae.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L3	8	koh near kwang-wook.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L4	50	kim near sang-su.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
5	BRS	L5	61	kim near jin-hee.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L6	24	kim near sung-ho.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L7	35	kim near ki-chul.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L8	1583	(ono) near25 (substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
9	BRS	L9	372	((ono) near25 (substrate)) near25 (polysilicon)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
10	BRS	L10	6	((ono) near25 (substrate)) near25 (polysilicon) near25 (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
11	BRS	L11	0	((ono) near25 (substrate)) near25 (poly-silicon) near25 (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
12	BRS	L12	0	((ono) near25 (substrate)) near25 (poly$5) near25 (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
13	BRS	L13	0	((oxide-nitride-oxide) near25 (substrate)) near25 (poly$5) near25 (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
14	BRS	L14	114	((oxide-nitride-oxide or ono) near25 (substrate)) near25 (poly$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
15	BRS	L15	17	((oxide-nitride-oxide or ono) near25 (wafer)) near25 (poly$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
16	BRS	L16	1671	((oxide-nitride-oxide or ono) near25 (substrate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
17	BRS	L17	448	(pattern$3 or etch$3 or remov$3) near15 ((oxide-nitride-oxide or ono) near25 (substrate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
18	BRS	L18	62	(pattern$3 or etch$3 or remov$3) near15 ((oxide-nitride-oxide or ono) near25 (wafer))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
19	BRS	L19	843	(pattern$3 or etch$3 or remov$3) near15 ((oxide-nitride-oxide or ono) near25 (polysilicon))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
20	BRS	L20	2073	(pattern$3 or etch$3 or remov$3) near15 (oxide-nitride-oxide or ono)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
21	BRS	L21	4	(pattern$3 or etch$3 or remov$3) near15 (oxide-nitride-oxide or ono) near25 (ldd)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
22	BRS	L22	9	(pattern$3 or etch$3 or remov$3) near15 (oxide-nitride-oxide or ono) near25 (doped near drain)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
23	BRS	L23	8	((oxide-nitride-oxide or ono) near25 (substrate)) near25 (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
24	BRS	L24	0	((oxide-nitride-oxide or ono) near25 (wafer)) near25 (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
25	BRS	L25	0	((oxide-nitride-oxide or ono) near25 (wafer)) same (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
26	BRS	L26	33	((oxide-nitride-oxide or ono) near25 (substrate)) same (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
27	BRS	L27	174	((oxide-nitride-oxide or ono) near25 (substrate)) and (split)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	U	1	Document ID	Title
1			US 20050029574 A1	Self-aligned 1 bit local SONOS memory cell and method of fabricating the same
2			US 20050014333 A1	Method for manufacturing a semiconductor device
3			US 20040241948 A1	Method of fabricating stacked gate dielectric layer
4			US 20010044184 A1	Nonvolatile semiconductor memory device and method of manufacturing the same
5			US 6590254 B2	Nonvolatile semiconductor memory device and method of manufacturing the same
6			US 6177316 B1	Post barrier metal contact implantation to minimize out diffusion for NAND device
7			US 20050029574 A	Fabrication of self-aligned 1 bit silicon oxide nitride oxide silicon memory cell, by etching portions of upper oxide layer and nitride layer of oxygen-nitride-oxide layer on insulating layer pattern, using self-aligned etching spacers
8			US 20040152286 A	Manufacture of non-volatile memory, e.g. random access memory, of silicon-oxide-nitride-oxide-silicon structure, by removing flash device and logic gate areas on which flash device and logic gate are formed, and forming lightly doped drain
9	X		US 5877523 A	Multilevel split-gate flash memory cell